The George Washington University

Department of Electrical and Computer Engineering

ECE 2140: Design of Logic Systems I

Final Projects

Revised Spring 2015

Objectives

The goal of your final project is to reuse the knowledge you have acquired during the semester to realize a complete project. You will have to go through (and document) all the phases of the conception (specification, architecture design, detailed design, implementation and tests). **Projects are to be realized strictly individually. Remember, GW's Academic Integrity Code still applies.**

The project will be based on the **Digilent Basys 2 Xilinx** boards. The boards are available in the Tech Center on the 5th floor of SEH. You will need to check the board out by using your Gworld ID and return the board every time you finish. Please keep in mind that you won't be able to borrow a board to use outside of lab. You will have to test your code using the **Xilinx ISE** simulation tool. (The design will still be tested on the board during the presentation). The due date for the report is **May 1st, 2015** (**on Blackboard**). But you will have to make a 5 minute presentation and a 3 minute demonstration of the working design during the last laboratory section.

Project Report Format

- Introduction
- Specifications
- Design
    - Overview
    - Schematics
- Implementation
    - Overview/Procedure
    - Verilog source code (must be in TEXT form, not an image of the code)
    - Simulation (if necessary)
    - Results
- Conclusion

Choose 1 of the following projects:

1. Chronograph

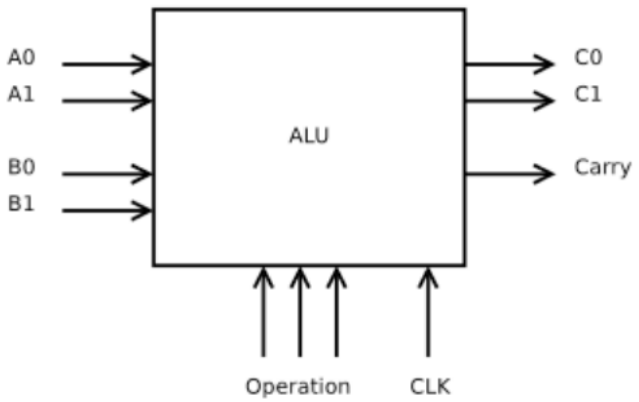
On the Digilent Basys2 FPGA board, design a chronograph. It should have the following functionality:

A. Seconds display on the LEDs (Extra Credits: Seconds Display on the Seven-Segment Displays)
B. Start/Stop switch
C. Reset/hold switch – if pressed while time is running, will freeze time displayed on LEDs (while still counting time in the background). After switch is moved back, the LEDs will display current time. If pressed while time is NOT running, will reset timer back to 0.

2. Two-bit Arithmetic Logic Unit (ALU)

Design a two-bit ALU in Verilog. Implement it on the Digilent Basys 2 FPGA board. Build a test circuit (testbench in verilog) for it. The ALU should have the following functionalities as listed in the table. (Extra Credits: Show Results on the Seven-Segment Displays)

Operation	Operation code	Result
Left shift	000	$C = A_0 0,\ Carry = A_1$
Right shift	001	$C = 0A_1,\ Carry = 0$
Addition	010	$C = A + B$
Substraction	011	$C = A - B$
XOR	100	$C = A\ xor\ B$
Or	101	$C = A\ or\ B$
And	110	$C = A\ and\ B$
Set	111	$C = 11,\ Carry = 1$



3. Choose Your Own Topic

You are also encouraged to design a project topic by yourself other than the topics that are given above. However, before you begin the project, you need to submit a brief proposal to your GTA for approval. The project you design should be based on the Digilent Basys 2 FPGA board.

Extra Credits (After you finish the Basys 2 project):

Build a one-digit counter using discrete integrated circuit (IC) components. Result must be displayed using seven-segment displays.